

256K (32K x 8) Static RAM

Features

■ Temperature Ranges

□ Commercial: 0°C to 70°C
□ Industrial: −40°C to 85°C
□ Automotive-A: −40°C to 85°C
□ Automotive-E: −40°C to 125°C

■ Speed: 70 ns

■ Low Voltage Range: 2.7V to 3.6V

■ Low Active Power and Standby Power

■ Easy Memory Expansion with CE and OE Features

■ TTL Compatible Inputs and Outputs

■ Automatic Power Down when Deselected

■ CMOS for Optimum Speed and Power

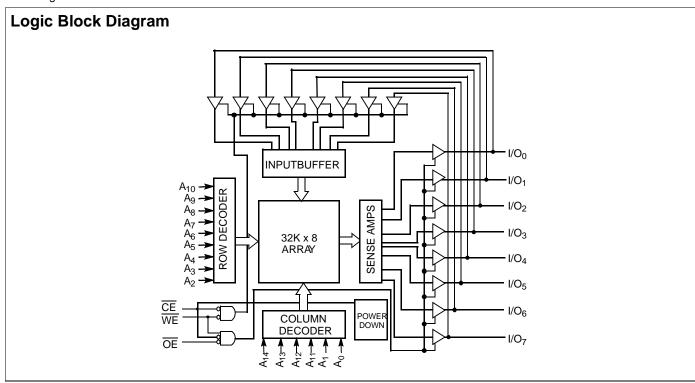
 Available in Standard Pb-free and non Pb-free 28-Pin (300-mil) Narrow SOIC, 28-Pin TSOP-I, and 28-Pin Reverse TSOP-I Packages

Functional Description

The CY62256VN^[1] family is composed of two high performance CMOS static RAM's organized as 32K words by 8 bits. Easy memory expansion is provided by an <u>active LOW</u> chip enable (CE) and active LOW output enable (OE) and tristate drivers. These devices have an automatic power down feature, reducing the power consumption by over 99% when deselected.

An active LOW write enable signal (WE) \underline{con} trols \underline{the} writing/reading operation of the memory. When \overline{CE} and \overline{WE} inputs are both LOW, data on the eight data input/output pins (I/O₀ through I/O₇) is written into the memory location addressed by the address present on the address pins (A₀ through A₁₄). Reading the device is $\underline{accomplished}$ by selecting the \underline{device} and enabling the outputs, \overline{CE} and \overline{OE} active LOW, while \overline{WE} remains inactive or HIGH. Under these conditions, the contents of the location addressed by the information on address pins are present on the eight data input/output pins.

The input/output pins remain in a high impedance state unless the chip is selected, outputs are enabled, and write enable (WE) is HIGH.



Note

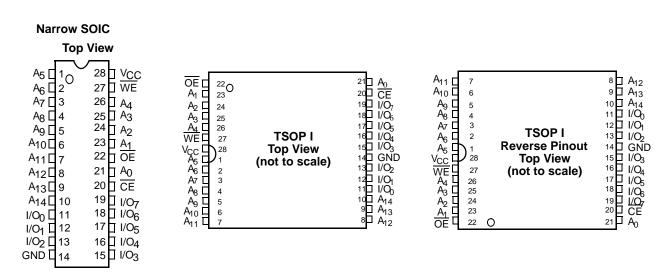
^{1.} For best practice recommendations, refer to the Cypress application note "System Design Guidelines" on http://www.cypress.com.



Product Portfolio

		V	. Pango /	W	Power Dissipation			
Product	Range	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	_{CC} Range (, v)	Operating, I _{CC} (mA)		Standby,	I _{SB2} (μA)
		Min	Typ ^[2]	Max	Typ ^[2]	Max	Typ ^[2]	Max
CY62256VNLL	Com'l	2.7	3.0	3.6	11	30	0.1	5
CY62256VNLL	Ind'I	2.7	3.0	3.6	11	30	0.1	10
CY62256VNLL	Automotive-A	2.7	3.0	3.6	11	30	0.1	10
CY62256VNLL	Automotive-E	2.7	3.0	3.6	11	30	0.1	130

Pin Configurations



Pin Definitions

Pin Number	Туре	Description
1–10, 21, 23–26	Input	A ₀ -A ₁₄ . Address Inputs
11–13, 15–19	Input/Output	I/O ₀ -I/O ₇ . Data lines. Used as input or output lines depending on operation
27	Input/Control	WE. When selected LOW, a WRITE is conducted. When selected HIGH, a READ is conducted
20	Input/Control	CE. When LOW, selects the chip. When HIGH, deselects the chip
22	Input/Control	OE. Output Enable. Controls the direction of the I/O pins. When LOW, the I/O pins behave as outputs. When deasserted HIGH, I/O pins are tristated, and act as input data pins
14	Ground	GND. Ground for the device
28	Power Supply	V _{CC} . Power supply for the device

Note

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^{2.} Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC} Typ, T_A = 25°C, and t_{AA} = 70 ns.



Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature-65°C to + 150°C Ambient Temperature with Power Applied–55°C to + 125°C Supply Voltage to Ground Potential (Pin 28 to Pin 14).....-0.5V to + 4.6V DC Input Voltage^[3] -0.5V to V_{CC} + 0.5V Output Current into Outputs (LOW)......20 mA

Static Discharge Voltage	. > 2001V
(per MIL-STD-883, Method 3015)	
Latch-up Current	> 200 mA

Operating Range

Device	Range	Ambient Temperature (T _A) ^[4]	V _{cc}
CY62256VN	Commercial	0°C to +70°C	2.7V to 3.6V
	Industrial	-40°C to +85°C	
	Automotive-A	-40°C to +85°C	
	Automotive-E	-40°C to +125°C	

Electrical Characteristics Over the Operating Range

Parameter	Decerintian	Test Conditions			-70			
Farailletei	Description	rest Condition	Min	Typ ^[2]	Max	Unit		
V _{OH}	Output HIGH Voltage	I _{OH} = −1.0 mA	V _{CC} = 2.7V	2.4			V	
V_{OL}	Output LOW Voltage	I _{OL} = 2.1 mA	V _{CC} = 2.7V			0.4	V	
V _{IH}	Input HIGH Voltage			2.2		V _{CC} + 0.3V	V	
V _{IL}	Input LOW Voltage			-0.5		0.8	V	
I _{IX}	Input Leakage Current	$GND \leq V_{IN} \leq V_{CC}$	Com'I/Ind'I/Auto-A	-1		+1	μА	
			Auto-E	-10		+10	μА	
I _{OZ}	Output Leakage Current	$GND \le V_{IN} \le V_{CC}$, Output	Com'I/Ind'I/Auto-A	-1		+1	μА	
		Disabled	Auto-E	-10		+10	μА	
I _{CC}	V _{CC} Operating Supply Current	$V_{CC} = 3.6V, I_{OUT} = 0 \text{ mA},$ $f = f_{MAX} = 1/t_{RC}$	All Ranges		11	30	mA	
I _{SB1}	Automatic CE Power Down Current - TTL Inputs	$V_{CC} = 3.6V, \overline{CE} \ge V_{IH},$ $V_{IN} \ge V_{IH} \text{ or } V_{IN} \le V_{IL}, f = f_{MAX}$	All Ranges		100	300	μА	
I _{SB2}	Automatic CE Power	$V_{CC} = 3.6V, \overline{CE} \ge V_{CC} - 0.3V$	Com'l		0.1	5	μА	
	Down Current- CMOS Inputs	$V_{IN} \ge V_{CC} - 0.3V \text{ or } V_{IN} \le 0.3V,$ f = 0	Ind'I/Auto-A			10		
	mpato		Auto-E			130		

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^{3.} V_{IL} (min) = -2.0V for pulse durations of less than 20 ns. 4. T_A is the "Instant-On" case temperature.



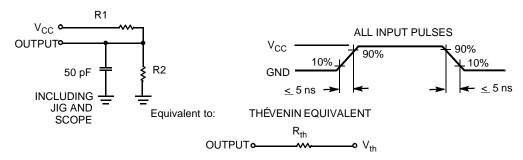
Capacitance^[5]

Parameter	Description	Test Conditions	Max	Unit
C _{IN}	Input Capacitance	$T_A = 25^{\circ}C$, $f = 1 \text{ MHz}$,	6	pF
C _{OUT}	Output Capacitance	$V_{CC} = 3.0V$	8	pF

Thermal Resistance^[5]

Parameter	Description	Test Conditions	SOIC	TSOPI	RTSOPI	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)	Still Air, soldered on a 3 × 4.5 inch, two-layer printed circuit board	68.45	87.62	87.62	°C/W
ΘJC	Thermal Resistance (Junction to Case)		26.94	23.73	23.73	°C/W

Figure 1. AC Test Loads and Waveforms

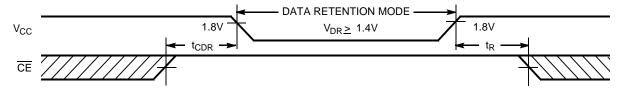


Parameter	Value	Units
R1	1100	Ohms
R2	1500	Ohms
RTH	645	Ohms
VTH	1.750	Volts

Data Retention Characteristics (Over the Operating Range)

Parameter	Description	Conditions ^[6]	Min	Typ ^[2]	Max	Unit	
V_{DR}	V _{CC} for Data Retention			1.4			V
I _{CCDR}	Data Retention Current	$\frac{V_{CC}}{V_{CC}} = 1.4V$	Com'l		0.1	3	μΑ
		$\begin{split} &\frac{V_{CC}}{CE} = 1.4 \text{V}, \\ &CE \geq V_{CC} - 0.3 \text{V}, \\ &V_{IN} \geq V_{CC} - 0.3 \text{V} \\ &\text{or } V_{IN} \leq 0.3 \text{V} \end{split}$	Ind'I/Auto-A			6	
		or V _{IN} ≤ 0.3V	Auto-E			50	
t _{CDR} ^[6]	Chip Deselect to Data Retention Time			0			ns
t _R ^[5]	Operation Recovery Time			t _{RC}			ns

Figure 2. Data Retention Waveform



Notes

- 5. Tested initially and after any design or process changes that may affect these parameters.
 6. No input may exceed V_{CC} + 0.3V.

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Switching Characteristics Over the Operating Range^[7]

Donomotor	Description	CY62256VN-70		
Parameter	Description	Min	Max	Unit
Read Cycle	·			•
t _{RC}	Read Cycle Time	70		ns
t _{AA}	Address to Data Valid		70	ns
t _{OHA}	Data Hold from Address Change	10		ns
t _{ACE}	CE LOW to Data Valid		70	ns
t _{DOE}	OE LOW to Data Valid		35	ns
t _{LZOE}	OE LOW to Low-Z ^[8]	5		ns
t _{HZOE}	OE HIGH to High-Z ^[8, 9]		25	ns
t _{LZCE}	CE LOW to Low-Z ^[8]	10		ns
t _{HZCE}	CE HIGH to High-Z ^[8, 9]		25	ns
t _{PU}	CE LOW to Power Up	0		ns
t _{PD}	CE HIGH to Power Down		70	ns
Write Cycle ^[10, 11]	·	<u>.</u>		
t _{WC}	Write Cycle Time	70		ns
t _{SCE}	CE LOW to Write End	60		ns
t _{AW}	Address Setup to Write End	60		ns
t _{HA}	Address Hold from Write End	0		ns
t _{SA}	Address Setup to Write Start	0		ns
t _{PWE}	WE Pulse Width	50		ns
t _{SD}	Data Setup to Write End	30		ns
t _{HD}	Data Hold from Write End	0		ns
t _{HZWE}	WE LOW to High-Z ^[8, 9]		25	ns
t _{LZWE}	WE HIGH to Low-Z ^[8]	10		ns

Notes

Test conditions assume signal transition time of 5 ns or less timing reference levels of V_{CC}/2, input pulse levels of 0 to V_{CC}, and output loading of the specified I_{OL}/I_{OH} and 100-pF load capacitance.
 At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
 t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with C_L = 5 pF as in (b) of <u>AC</u> Test Loads. Transition is measured ± 200 mV from steady-state voltage.
 The internal write time of the memory is defined by the overlap of CE LOW and WE LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
 The minimum write cycle time for write cycle #3 (WE controlled, OE LOW) is the sum of t_{HZWE} and t_{SD}.



Switching Waveforms

Figure 3. Read Cycle No. 1^[12, 13]

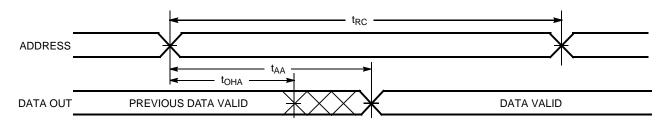


Figure 4. Read Cycle No. 2^[13, 14]

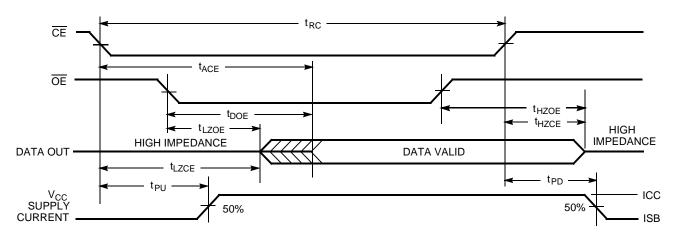
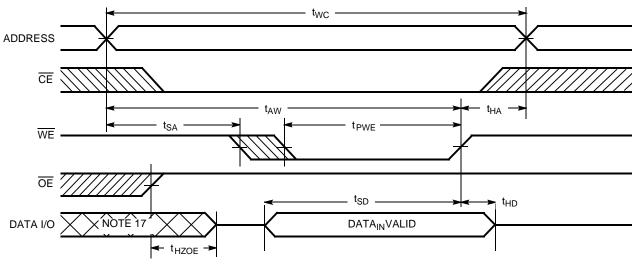


Figure 5. Write Cycle No. 1 (WE Controlled)[10, 15, 16]



- 12. Device is continuously selected. \overline{OE} , $\overline{CE} = V_{IL}$.
- 13. WE is HIGH for read cycle.
- 14. Address valid prior to or coincident with $\overline{\text{CE}}$ transition LOW.
- 15. Data I/O is high impedance if $\overline{\text{OE}} = \text{V}_{\text{IH}}$.

 16. If $\overline{\text{CE}}$ goes HIGH simultaneously with WE HIGH, the output remains in a high impedance state.
- 17. During this period, the I/Os are in output state and input signals should not be applied.

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Switching Waveforms (continued)

Figure 6. Write Cycle No. 2 ($\overline{\text{CE}}$ Controlled)[10, 15, 16]

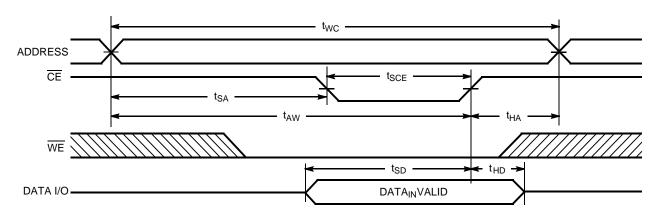
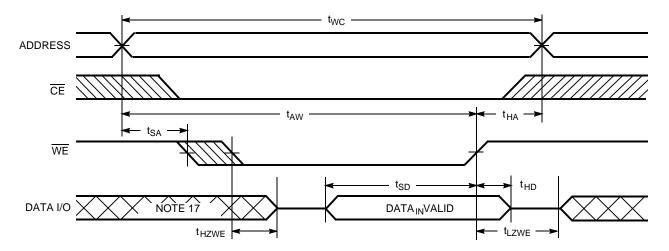


Figure 7. Write Cycle No. 3 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ LOW)[11, 16]

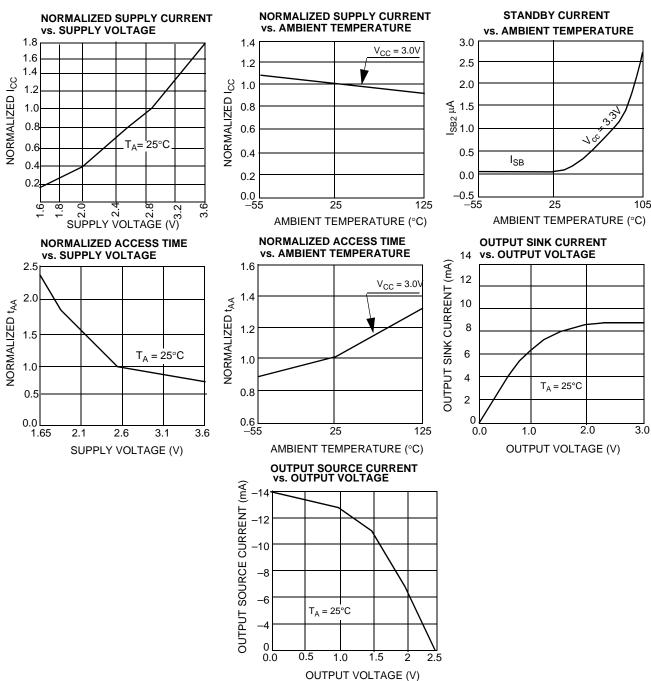


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[+] Feedback



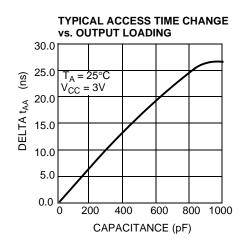
Typical DC and AC Characteristics

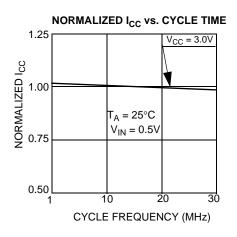


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Typical DC and AC Characteristics (continued)





Truth Table

CE	WE	OE	Inputs/Outputs	Mode	Power
Н	Х	Х	High-Z	Deselect/Power Down	Standby (I _{SB})
L	Н	L	Data Out	Read	Active (I _{CC})
L	L	Х	Data In	Write	Active (I _{CC})
L	Н	Н	High-Z	Deselect, Output Disabled	Active (I _{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
70	70 CY62256VNLL-70SNC 51-85092 28-Pin (3		28-Pin (300-mil) Narrow SOIC	Commercial
	CY62256VNLL-70SNXC		28-Pin (300-mil) Narrow SOIC (Pb-Free)	
	CY62256VNLL-70ZC	51-85071	28-Pin TSOP I	
	CY62256VNLL-70ZXC		28-Pin TSOP I (Pb-Free)	
	CY62256VNLL-70SNXI	51-85092	28-Pin (300-mil) Narrow SOIC (Pb-Free)	Industrial
	CY62256VNLL-70ZI	51-85071	28-Pin TSOP I	
	CY62256VNLL-70ZXI		28-Pin TSOP I (Pb-Free)	
	CY62256VNLL-70ZRI	51-85074	28-Pin Reverse TSOP I	
	CY62256VNLL-70ZRXI		28-Pin Reverse TSOP I (Pb-Free)	
	CY62256VNLL-70ZXA	51-85071	28-Pin TSOP I (Pb-Free)	Automotive-A
	CY62256VNLL-70SNXE	51-85092	28-Pin (300-mil) Narrow SOIC (Pb-Free)	Automotive-E
	CY62256VNLL-70ZXE	51-85071	28-Pin TSOP I (Pb-Free)	
	CY62256VNLL-70ZRXE	51-85074	28-Pin Reverse TSOP I (Pb-Free)	

Contact your local Cypress sales representative for availability of other parts

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Package Diagrams

Figure 8. 28-Pin (300-mil) SNC (Narrow Body) (51-85092)

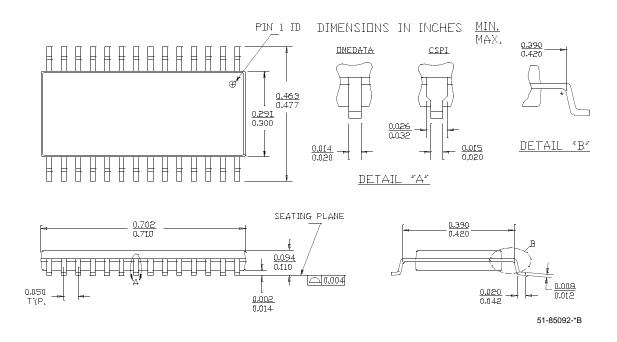
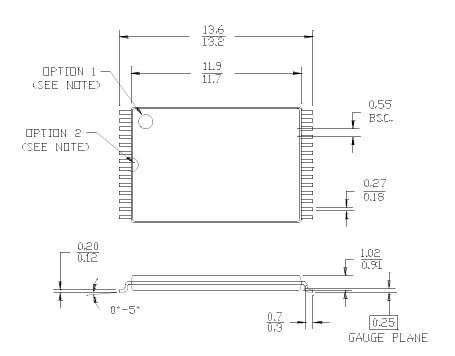
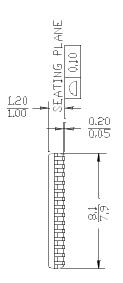




Figure 9. 28-Pin TSOP 1 (8 x 13.4 mm) (51-85071)

NDTE: ORIENTATION I.D MAY BE LOCATED EITHER AS SHOWN IN OPTION 1 OR OPTION 2





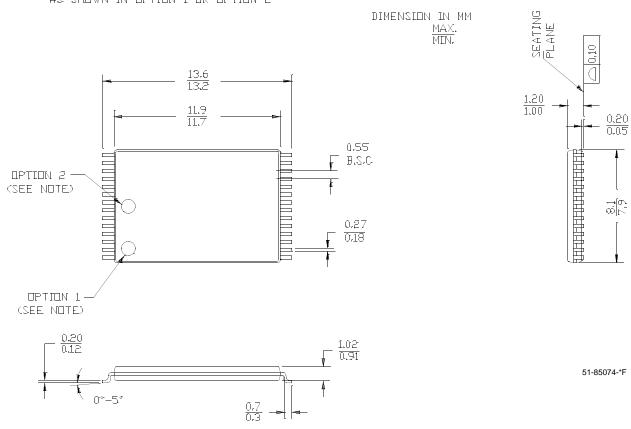
 $\begin{array}{c} \text{DIMENSION IN MM} \\ \frac{\text{MAX.}}{\text{MIN.}} \end{array}$

51-85071-*G



Figure 10. 28-Pin Reverse TSOP 1 (8 x 13.4 mm) (51-85074)

NOTE: ORIENTATION I.D MAY BE LOCATED EITHER AS SHOWN IN OPTION 1 OR OPTION 2



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Document History Page

Document Title: CY62256VN 256K (32K x 8) Static RAM Document Number: 001-06512				
Rev.	ECN No.	Submission Date	Orig. of Change	Description of Change
**	426504	See ECN	NXR	New Data Sheet
*A	488954	See ECN		Added Automotive product Updated ordering Information table
*B	2769239	09/25/09	VKN/AESA	Corrected V _{IL} description in the Electrical Characteristics table

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